Computerized Tomography Meets the Challenges of IC Package Inspection

The demand for smaller and thinner devices is driving the development of complex semiconductor packages with 3D wire bonding and multiple-level solder-bump interconnections. Traditional inspection methods, however, are unable to inspect these packages adequately. This article discusses the benefits of computerized tomography for complex package inspection.

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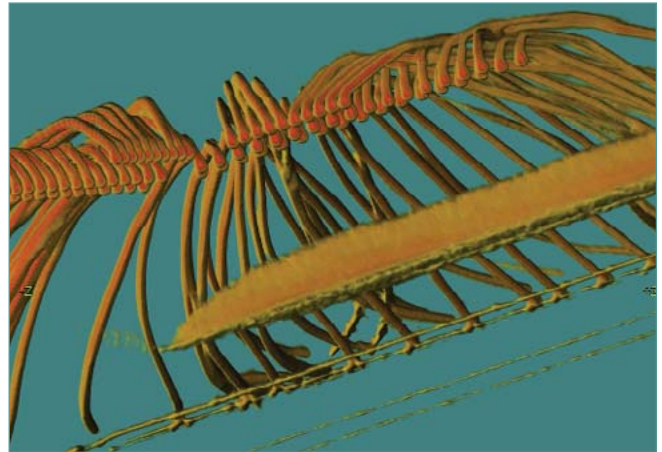

This CT image exhibits multi-level wire bonding within a stacked-die device, a defect type that typically can't be seen with 2D cross sectioning or 2D x-ray inspection.

Current electronics continue to decrease in size while yielding improved performance. At the same time, semiconductor packaging is evolving from traditional leadframe-based devices to more advanced 3D devices such as system-in-package (SiP) and stacked die.

Multi-function portable electronic products remain at the forefront in stimulatating demand for miniaturized chips. Complex multi-layer die and wire-bonded 3D packages are among the major drivers in semiconductor inspection technology.

Packaging Trends

Semiconductor design engineers continue to integrate SiPs with multiple stacked-die packages, package-in-package (PiP) and package-on-package (PoP). These devices typically contain multiple stacked die with multi-level wire bonding or wafer bumping internal to the device.

Current PoP design practice combines logic and memory stacked into a single device. The benefits of this package design scheme include high-density interconnects, extremely low device profiles and increased board-level reliability.

Final product size constraints typically require semiconductor packages with smaller footprints and lower profiles. At the same time, board-level interface and assembly processes continue to drive interconnect density.

This trend is forcing device integration into a single package and therefore argues for the use of subsystems while reducing the total number of I/O at the circuit board level.

Market Needs

These advanced 3D packages place a great demand on package inspection and qualification processes during final packaging, assembly and test.

Since many features within these packages are hidden between multiple layers, it is difficult to see defects or to conduct a comprehensive failure analysis with traditional methods such as 2D x-ray inspection and cross sectioning.

In addition, cross sectioning is a destructive technology that is both time consuming and expensive and results in the loss of the sample. Analysis using 2D x-ray inspection has the advantage of being a non-destructive technology, but is often limited with these new package types since all of the multiple layers within the device are seen at the same time.

The result may be confusing with the multiple dies and multiple layers of wire bonds appearing to overlap each other within a 2D image. A failure analysis tool was needed that would allow the detection of hidden defects within complex packaging systems and subsystems (Figure 1).

Advances in computerized tomography (CT) have improved both imaging speed and resolution, enabling complete analysis of finite device features. Because of these improvements CT has become an appealing inspection methodology for advanced packages since it non-destructively generates a 3D model of the entire semiconductor package.

The resulting 3D model may be viewed in realtime so that interconnections normally obscured by other joints or components within the package can be diagnosed, assuring complete package inspection.

What is Computerized Tomography?

Computerized tomography is an imaging method where computational geometric processing is used to generate a 3D model of an object from a series of individual 2D x-ray images.

The CT model is developed by a computer from a series of 2D x-ray images taken as a semiconductor device is rotated within an x-ray beam. Variations in

Figure 1. CT machines are able to visualize anomalies such as delamination and voids in three dimensions. (Dage Precision Industries)

the material density represented by different grey levels within those images and how those change during rotation are reconstructed to produce a 3D model of the entire device.

The 3D model that is produced can be viewed and manipulated, providing an unlimited number of analytical images (or slices) through any plane within the model.

The components of producing a CT model include acquiring the necessary 2D x-ray images, computerized reconstruction from the 2D images into a CT model and the visualization and manipulation of the completed 3D model.

Acquisition of the 2D images takes place as a sample is fully rotated (360°) within a plane perpendicular to the axis of the x-ray tube and detector. The more steps that are taken during each degree of rotation, the greater the number of 2D images obtained, producing a higher quality CT model.

Image Acquisition

Acquiring the necessary images is the most time-consuming portion of the overall CT process and is directly related to the number of rotational steps that are used.

Each 2D x-ray image is produced by averaging the number of frames from

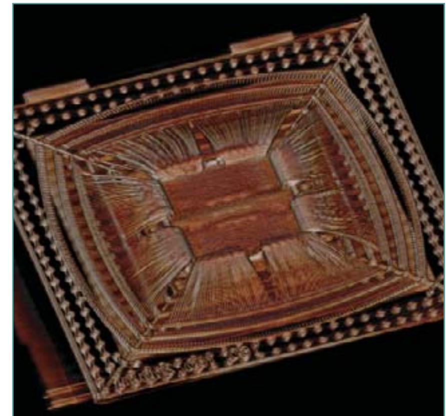

Figure 2. CT image of multi-level wire bonding within a stacked-die device

the realtime image capture of the x-ray system—usually an advanced digital image intensifier or a flat panel.

The number of frames averaged at each imaging step, the frame acquisition speed, and the number of steps govern the total acquisition speed. Reducing the number of steps or reducing the frame average per step will speed up the

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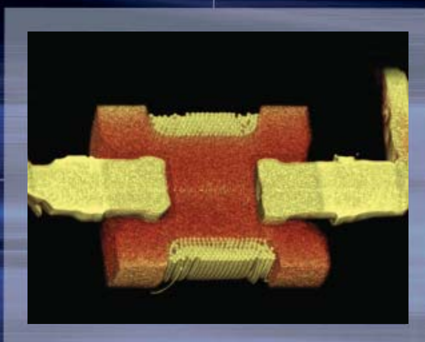

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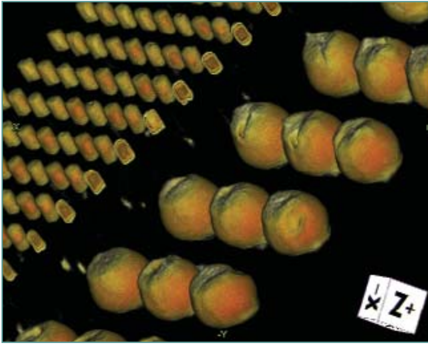


Figure 3. An image of a multi-layer device, viewed by CT, shows interfacial voiding in 400-micron BGA balls.

acquisition process but will reduce the quality of the 3D model.

The precision with which a sample is rotated during the image acquisition process is crucial to achieving a good reconstruction with high resolution. Without a high degree of precision, the ability of the CT reconstruction algorithm is greatly limited because the mathematical calculation requires that the density variation within each 2D image be tracked precisely during sample rotation.

3D Modeling

For some CT systems, the volume reconstruction process can be time consuming. Vast amounts of computer processing time are needed to calculate the density variation of each pixel in each image step and to work out how that density varies as the sample rotates.

In this way, the sample volume can be mapped out within a reconstructed 3D matrix, with its resolution defined in terms of volume pixels (voxels).

Advanced Software

The last element of the CT process is the advanced software that manipulates the reconstructed 3D model and facilitates visualization of the necessary 2D slices for the proper analytical view. This is the critical step that allows an end user to see the density contours within the CT model and to change how a particular slice is viewed.

In this manner, individual slices can be viewed through any plane in the CT model providing complete visualization of features within a device. Newer CT systems provide hardware accelerator graphics cards that specifically handle the manipulation and rendering of the CT model in real-time.

The 3D CT model can be viewed and manipulated separately and during image acquisition, allowing analysis of one CT model while the 2D images for another one are being collected.

CT Benefits

Because of the previously stated limitations of cross sectioning and 2D x-ray imaging, CT is increasingly used to inspect semiconductor devices for interconnection and die-attach quality, as well as wire bond integrity within complex 3D packages.

CT is a relatively new technology that offers 3D reconstruction of all internal elements of a packaged device and offers the benefits of being able to detect hidden defects, voiding within various device layers and density variations.

Recently developed CT systems offer visualization software with features that include image manipulation, image cropping, volume rendering, multiple cross sectional viewing of individual slices and creation of animated clips allowing a "flying trip" through the entire CT model.

In addition to analysis of interconnection and wire bond integrity within complex 3D packages, many of the newer CT systems can also perform high-resolution 2D inspection functions.

The user, therefore, has a common inspection platform which has the flexibility to rapidly and easily convert an x-ray system between 3D and 2D modes, thus satisfying all x-ray inspection needs. The latest advances in x-ray tube technology allow both 2D and 3D analysis with a high degree of grey scale sensitivity with feature recognition as

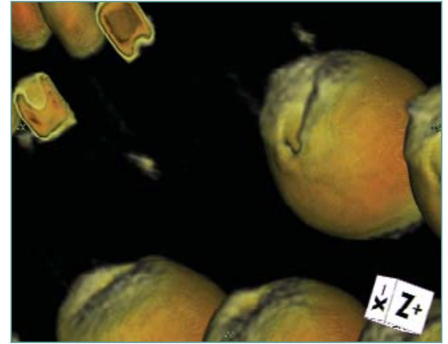


Figure 4. CT image of slice through solder bumps within a multi-layer interconnection showing interfacial voiding

fine as 250nm in 2D mode.

The best way to illustrate the differences between traditional 2D X-ray inspection and computerized tomography is to review several realworld semiconductor packaging inspection applications.

Wire Bond Integrity

As the number and layers of wire bonds increase within a stacked-die package, the ability to detect wire bond defects becomes even more important. Traditional analysis using 2D x-ray inspection is often limited with advanced packages since multiple layers within a device are seen at the same time.

This analysis can be confusing with the multiple dies and multiple layers of wire bonds appearing to overlap each other during the imaging process. (Figure 2 illustrates multiple wire bonds

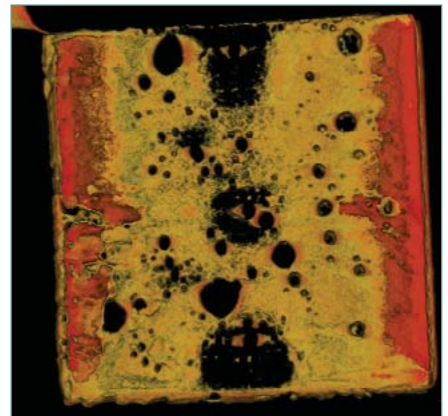


Figure 5. Slice of a power device, viewed by CT, reveals voiding and material density variation within heat transfer material

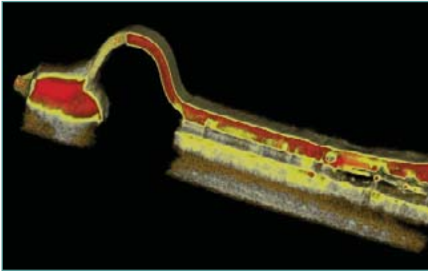


Figure 6. CT slice representing density variations and interlayer delamination within the thermal transfer layer of power device

within a stacked- die device.)

The use of CT allows the multiple layers of wire bonds to be represented in 3D so that the user can fly through the 3D model and easily detect defects. These anomalies may include the shape of bond wires as formed during the bonding process, wires touching the die, pads or other bond wires; and the detection of loose particles remaining from the bonding process that may cause potential signal interference or shorting. (Figure 2 shows multiple-level wire bonding.)

These types of wire bond defects typically cannot be detected with traditional 2D cross sectioning or 2D x-ray inspection.

Multi-Layer Interconnection

The increased use of complex, 3D packages results in more multi-layer interconnections within a single device. Often stacked die devices consist of multiple layers of silicon-based flip-chips and a multi-layer PWB carrier with multiple layers of solder bumps and solder-ball interconnections.

While the silicon die is difficult to image due to its low absorption of the x-rays, the interconnection circuitry consisting of multiple layers of solder bumps and solder balls is easily observed with x-ray.

However defects which are internal to these solder joints can be difficult to see using conventional 2D x-ray inspection since different layers are imaged at the same time and may obscure subtle features—especially within smaller objects.

The CT technique provides a new tool to look for hidden defects, such as interfacial voiding within solder bumps and BGA solder balls; as well as interfacial cracks and cracks in vias and circuitry paths.

Figure 3 shows a 3D model of a multi-layer device. Interfacial voiding is evident in the 400-micron diameter/700-micron pitch solder-ball joints. It would be difficult to determine the exact location of the voiding using conventional 2D X-ray examination.

Likewise, CT can be utilized to detect defects within solder bumps that could not otherwise be detected with a non-destructive method because of the complexity of the interconnections within the device.

The example in Figure 4 shows a slice through 100-micron solder bumps on a 250-micron pitch of the same multi-layered device. Interfacial voiding on both the bump-to-die and bump-to-substrate interfaces is apparent.

Voiding and Heat Transfer

Thermal transfer and heat dissipation are critical issues for discrete power devices, especially those used for high-current automotive electronics applications.

Voids within heat-transfer material can potentially cause a device to fail due to inadequate thermal transfer over the expected life of the end product. The location of the voiding is critical to heat dissipation characteristics and can be easily identified and exactly located using CT modeling.

A key point is that in using CT, one can precisely determine and separate the location of the various voids within the *x*, *y* and *z* planes of a device. When using conventional 2D x-ray all the voiding appears to be overlaid on top of each other.

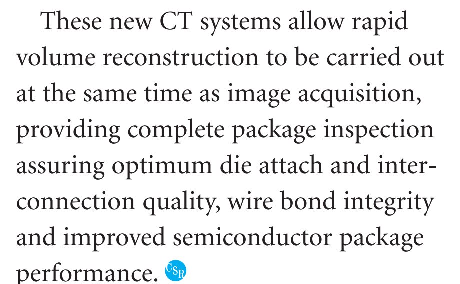
Figure 5 represents a CT slice through a heat transfer layer revealing significant voiding. By moving the "cutting plane" through the device, one can examine the voiding at different Z-axis levels.

Separation between the thermal transfer layer and the substrate within the assembly, together with internal voiding, can severely decrease the heat dissipation properties of a device.

Figure 6 represents a slice through a discrete power device in the perpendicular plane. Delamination, voiding, and material-density variations within the heat transfer layers are apparent. The use of destructive cross sectioning is particularly time consuming and expensive to identify internal defects such as voiding and delamination, an inspection operation easily performed by CT modeling.

Conclusion

While many manufacturing defects can be identified with 2D x-ray inspection, in numerous semiconductor packaging applications where interconnections within a device are obscured by other features, destructive analysis is required.



New advancements in computerized tomography make it an appealing technique for the inspection of advanced 3D packages and have reduced the necessity for destructive testing.

These new CT systems allow rapid volume reconstruction to be carried out at the same time as image acquisition, providing complete package inspection assuring optimum die attach and interconnection quality, wire bond integrity and improved semiconductor package performance.

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